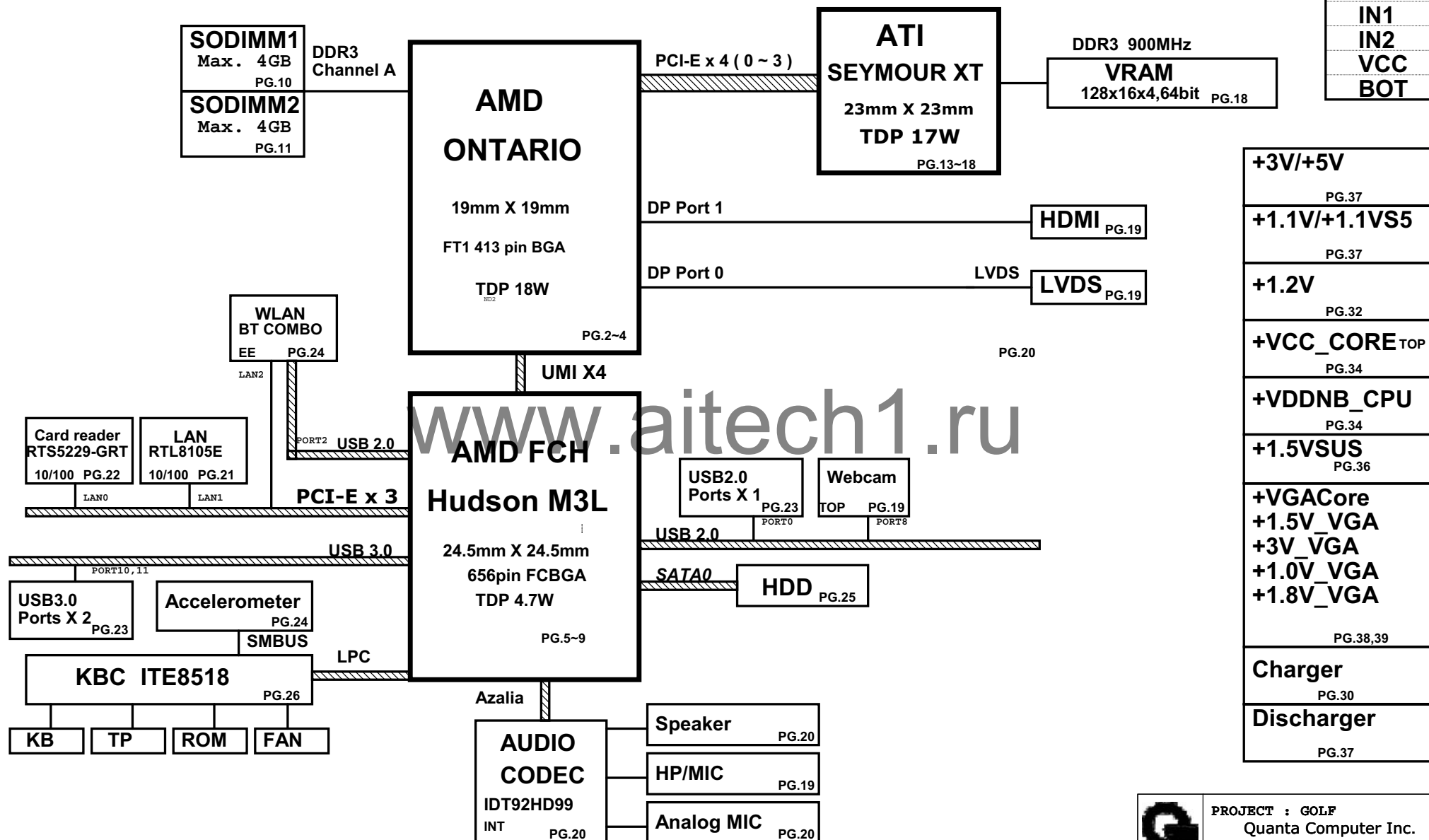


GOLF AMD UMA/Muxless SYSTEM DIAGRAM

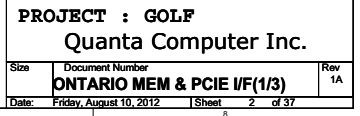
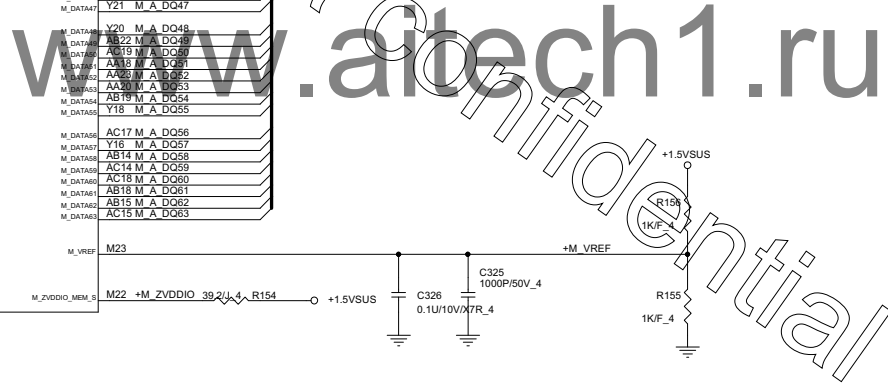
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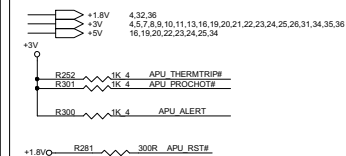
TOP
GND
IN1
IN2
VCC
BOT



PROJECT : GOLF
Quanta Computer Inc.

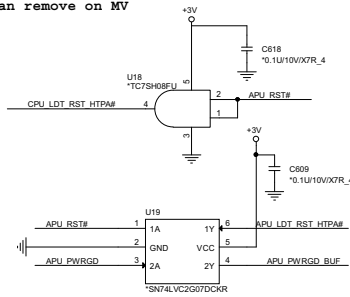
Size	Document Number	Rev
	Block Diagram	1A
Date:	Friday, August 10, 2012	Sheet 1 of 37



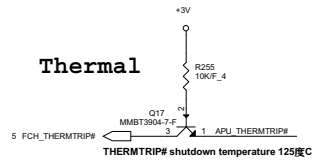


APU_PROCHOT#

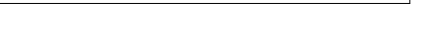
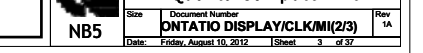
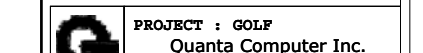
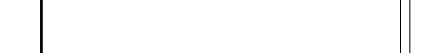
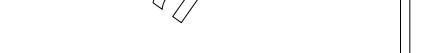
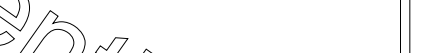
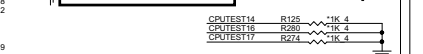
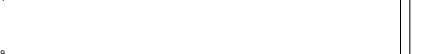
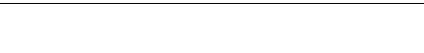
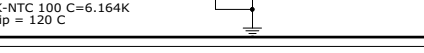
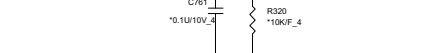
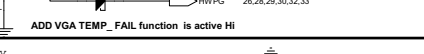
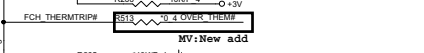
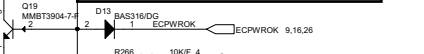
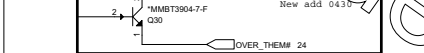
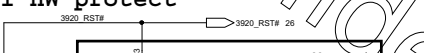
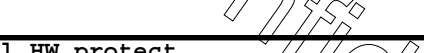
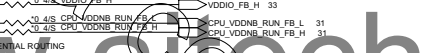
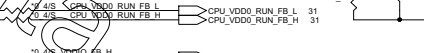
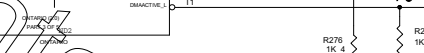
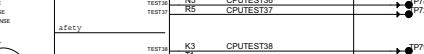
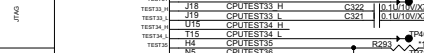
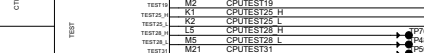
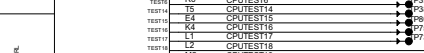
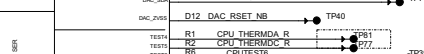
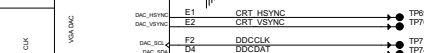
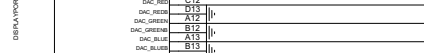
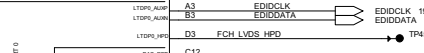
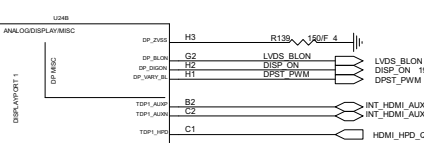
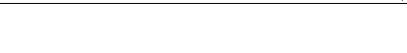
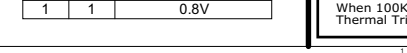
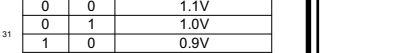
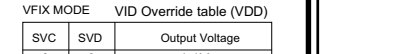
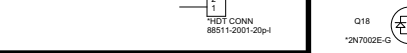
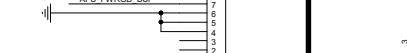
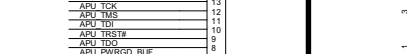
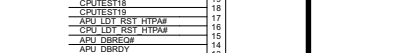
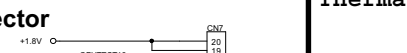
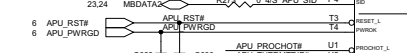
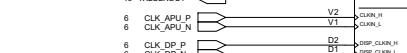
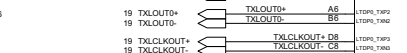
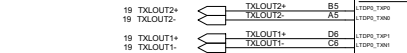
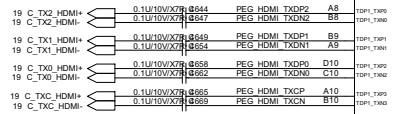
Can remove on MV



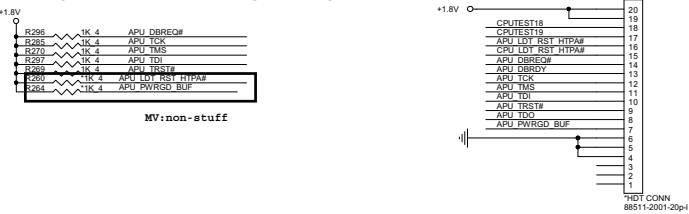
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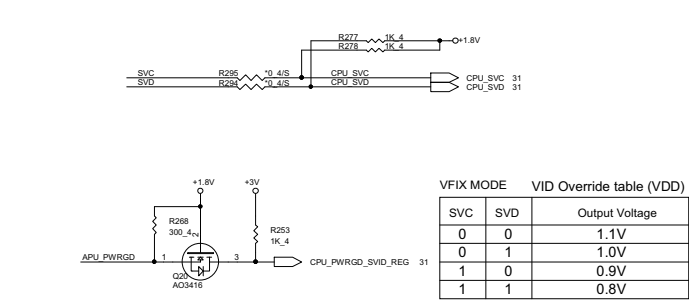
R52 DB ADD



HDT(Hardware Debug Tool) Connector



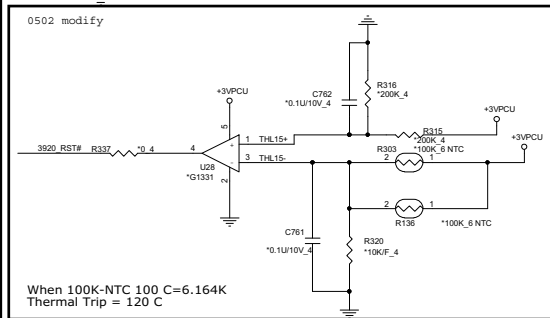
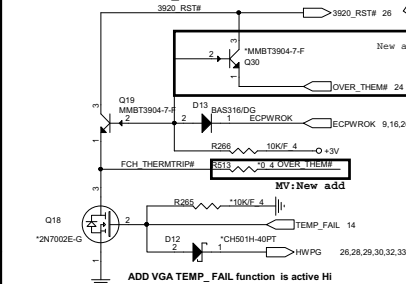
Serial VID



VFIX MODE VID Override table (VDD)

SVC	SVD	Output Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Thermal HW protect



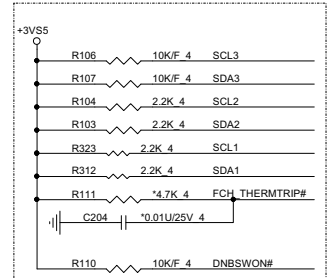
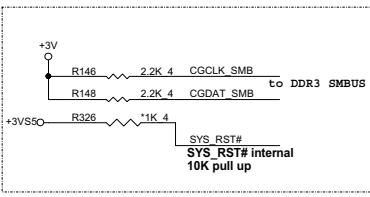
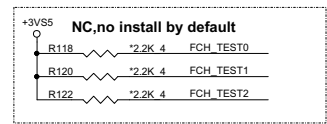
PROJECT : GOLF
Quanta Computer Inc.

Size Document Number
ONTATIO DISPLAY/CLK/M(2/3)

Date: Friday, August 10, 2012 1 Sheet 3 of 37

Rev 1A

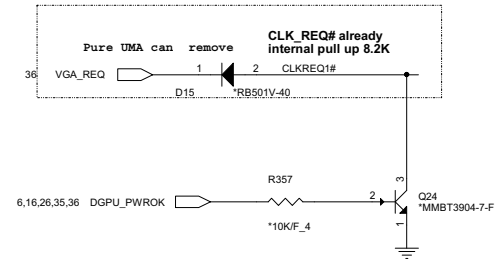
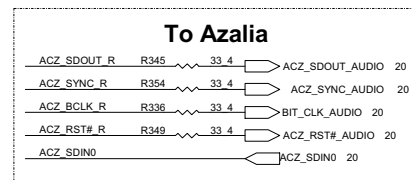




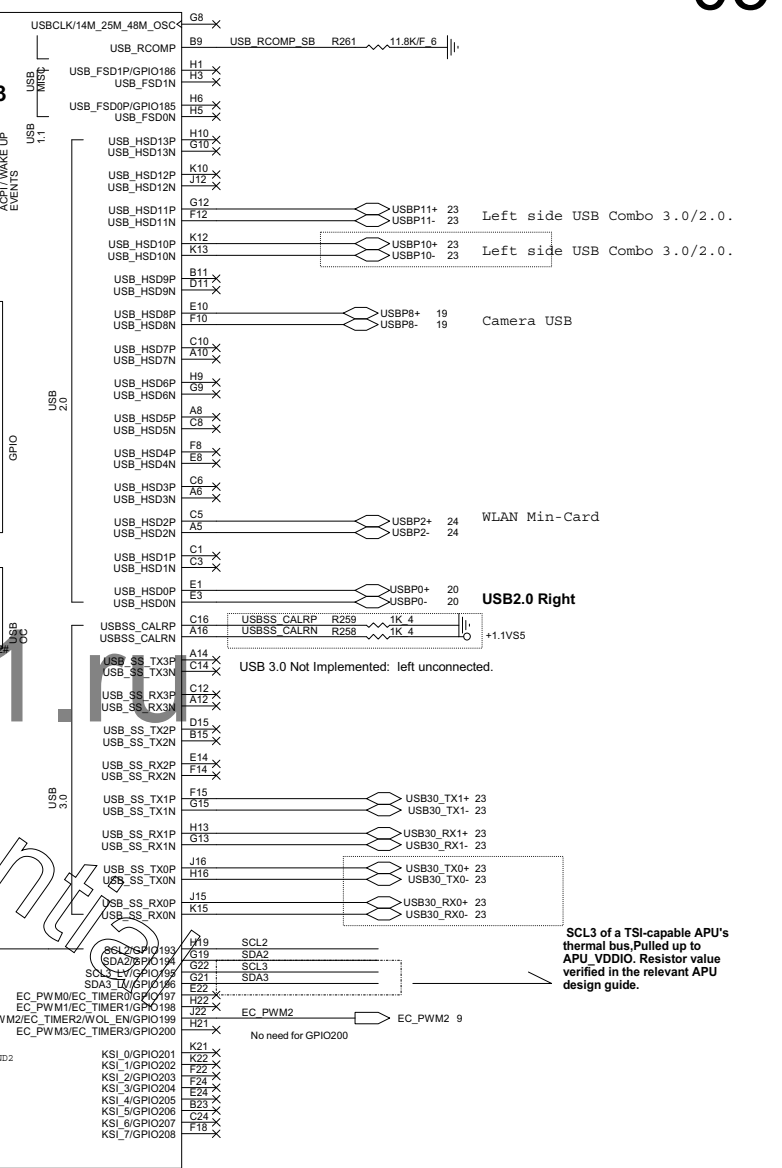
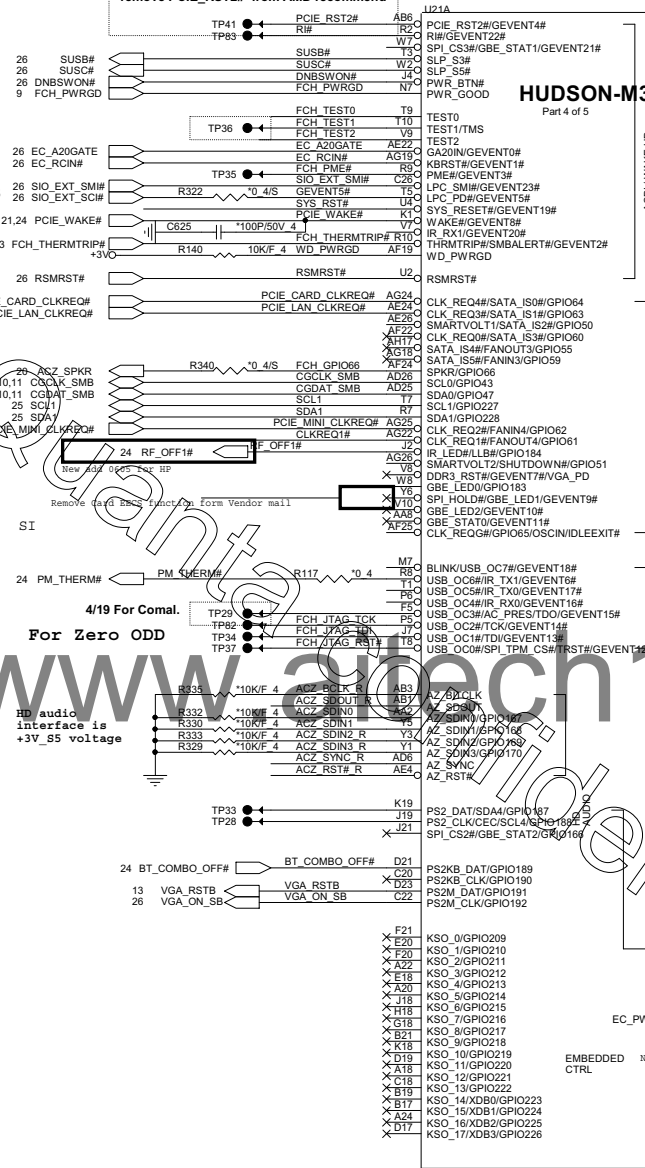
CLK_REQ2# internal pull Hi 8.2K to +3V
CLK_REQ3# internal pull Hi 8.2K to +3V
CLK_REQ4# internal pull Hi 8.2K to +3V

This pin is used to
power down VGA DAC
regulators when CRT
no connected

GEVENT16# internal pull Hi 8.2K to +3VS5
GEVENT15# internal pull Hi 8.2K to +3VS5



remove PCIE_RST2# from AMD recommend



SCL3 of a TSI-capable APU's
thermal bus. Pulled up to
APU_VDDIO. Resistor value
verified in the relevant APU
design guide.

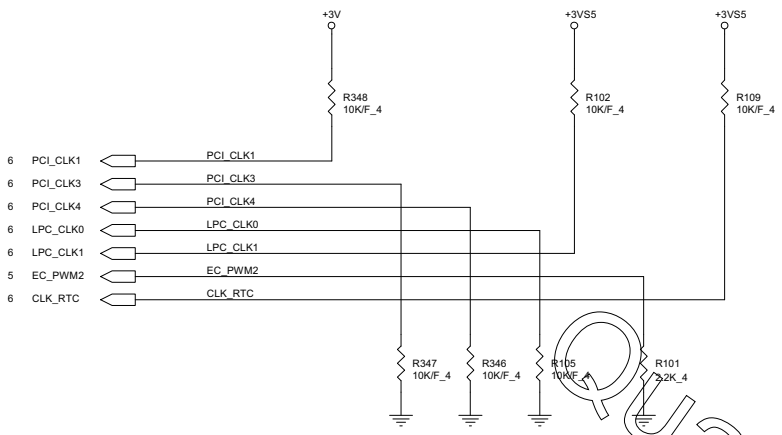
1007mA for M3
902mA for M2



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STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



REQUIRED STRAPS

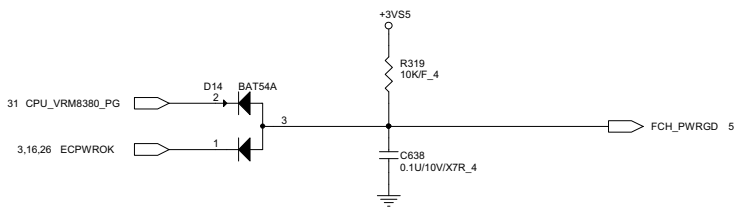
	*****	PCI_CLK1	*****	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	CLK_RTC
PULL HIGH	*****	ALLOW PCIe Gen2 DEFAULT	*****	USE DEBUG STRAP	non_Fusion CLOCK MODE	AMD internal EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM DEFAULT	\$S PLUS MODE ENABLED
PULL LOW	*****	FORCE PCIe Gen1	*****	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM	\$S PLUS MODE DISABLED DEFAULT

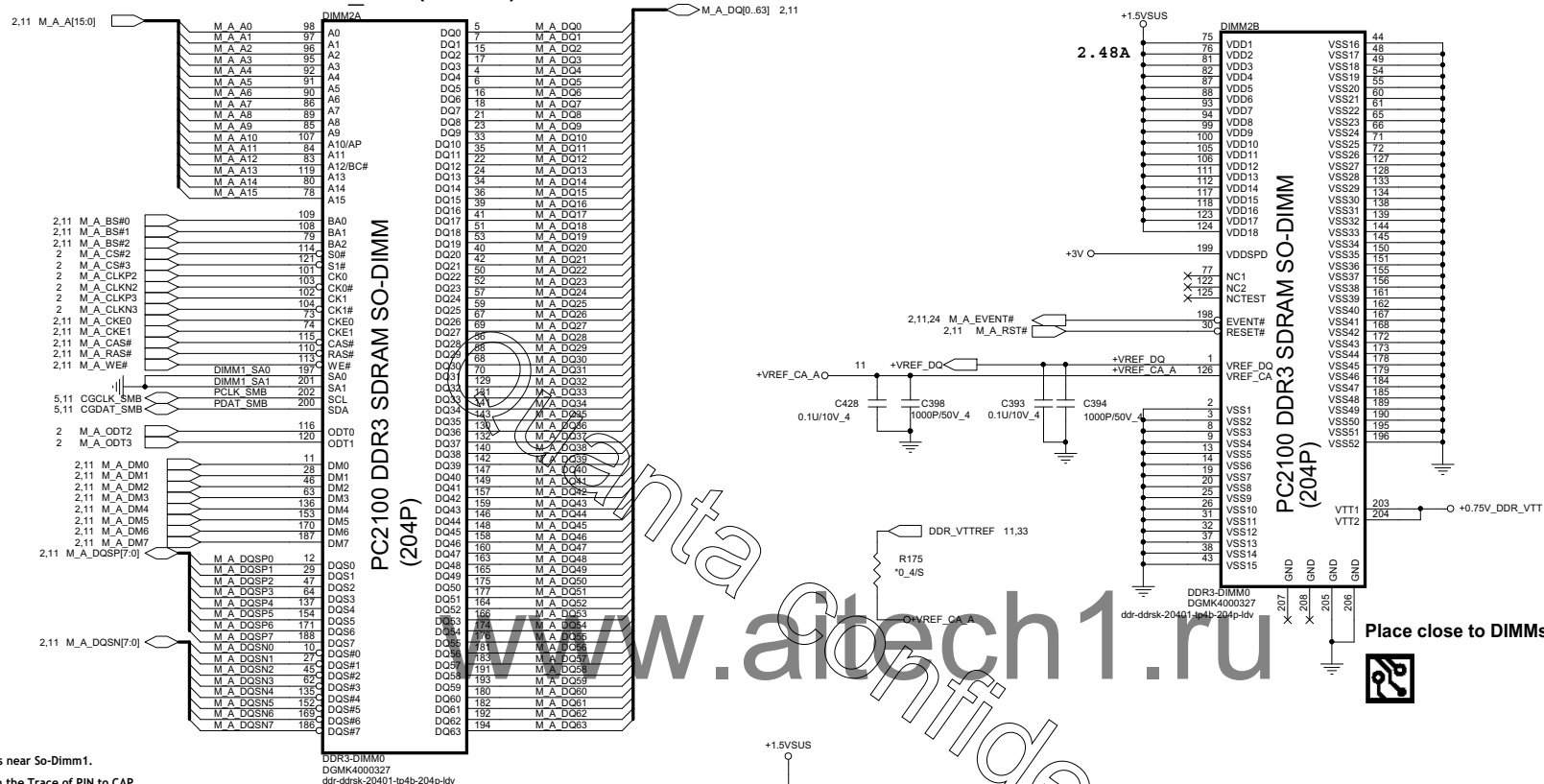
DEBUG STRAPS

FCH has 15K Internal Pull Up for PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIe STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIe STRAPS	ENABLE PCI MEM BOOT

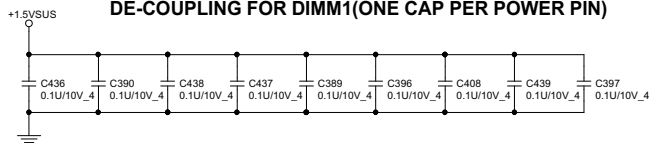
FCH PWRGD



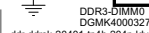
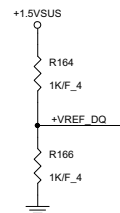


Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

DE-COUPLING FOR DIMM1(ONE CAP PER POWER PIN)



DE-COUPLING FOR DIMM1



Place close to DIMMs

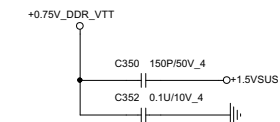
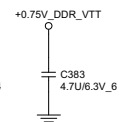
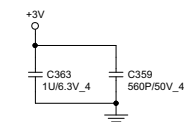
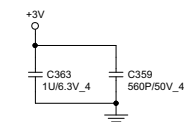


DIMM1A



No Vias Between the Trace of PIN to CAP.

DE-COUPLING FOR DIMM2



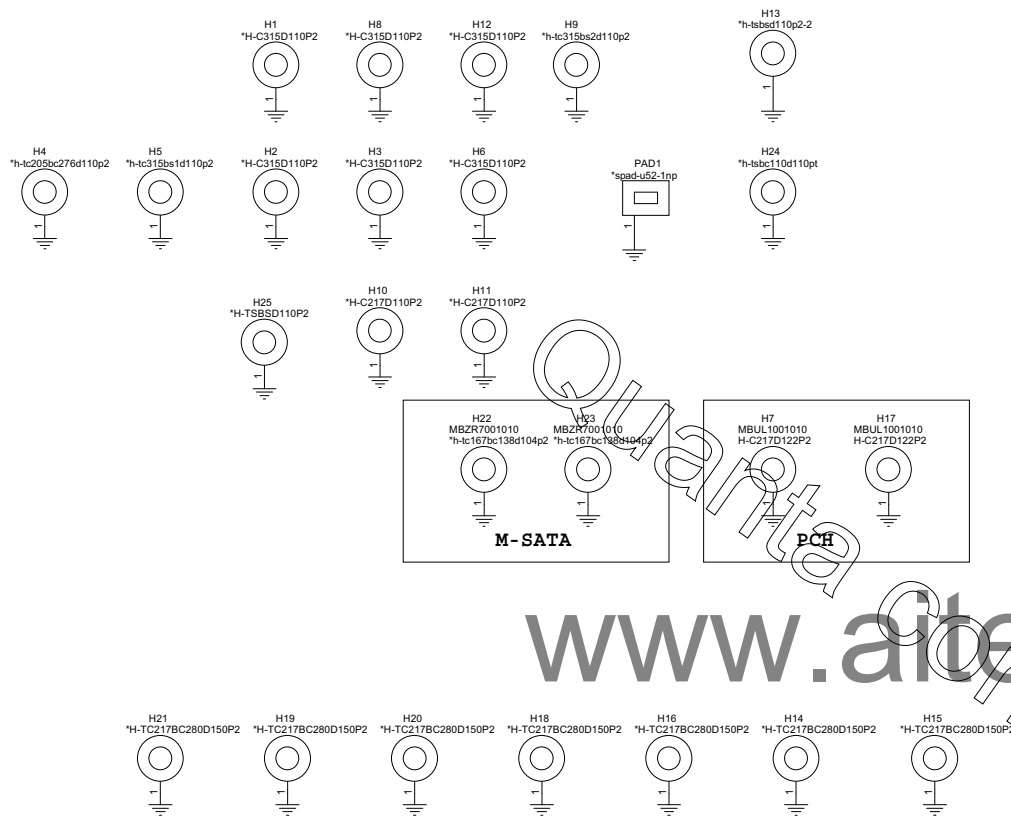
Return Path for DDR Plane

The diagram illustrates the return path for the DDR plane. It features a +1.5VSUS supply connected to a series of capacitors (C357, C338, C385, C360, C362) connected to ground. Each capacitor has a value of 0.1u/10V_4.



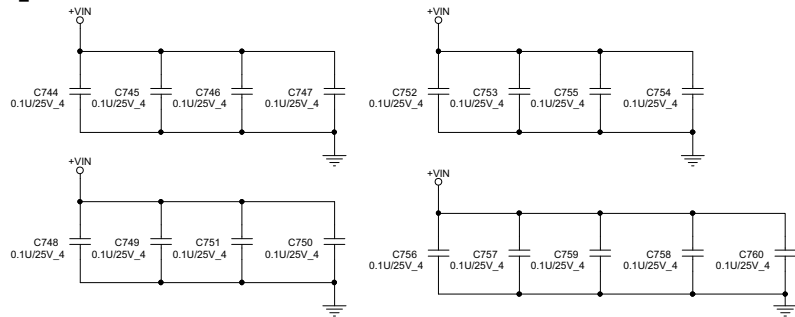
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+3V
R_VTT
5VSUS

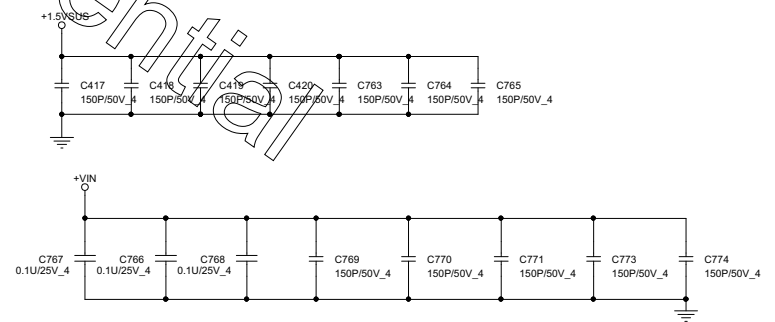


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Vin Cap

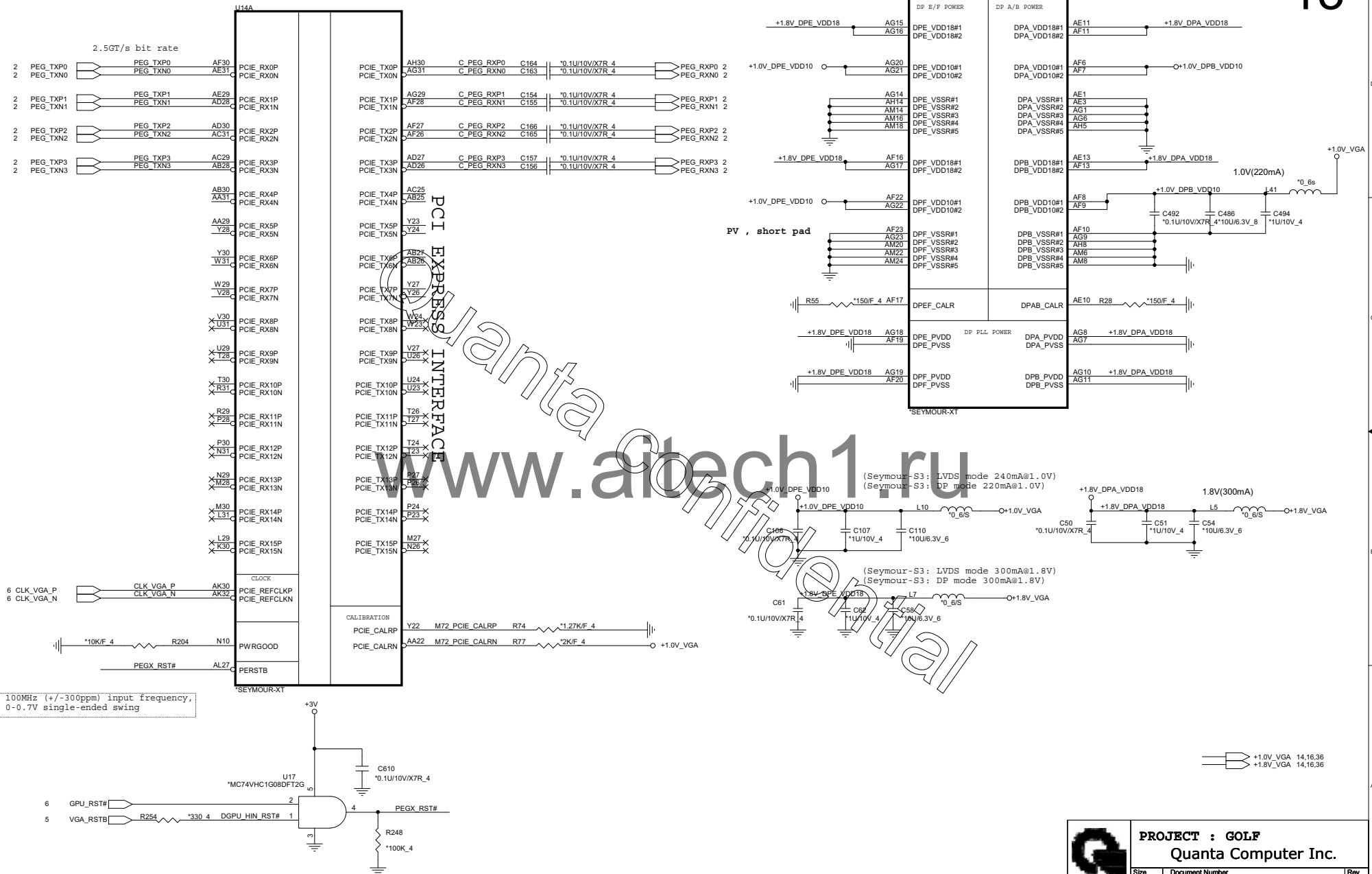


+1.5VSUS Cap for EMI 06/14 add



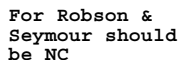
PROJECT : GOLF
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Size	Document Number	Rev
Custom	HOLE	1A
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PROJECT : GOLF
Quanta Computer Inc.

Size Custom Document Number **SEYMOUR-XT PCIE_Interface** Rev 1A
Date: Friday, August 10, 2012 Sheet 13 of 37

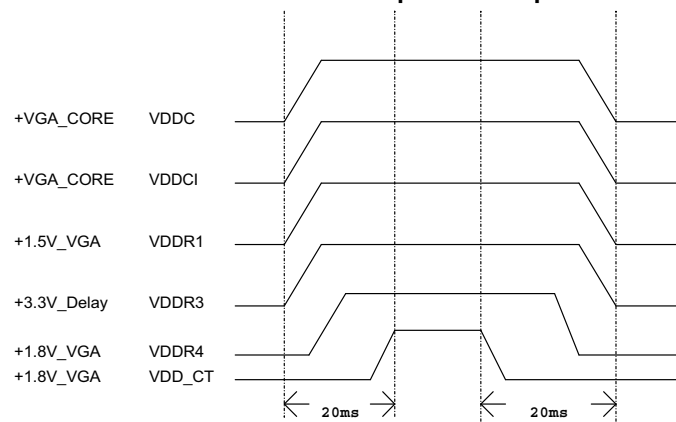


NOTE: AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

NOTE 1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

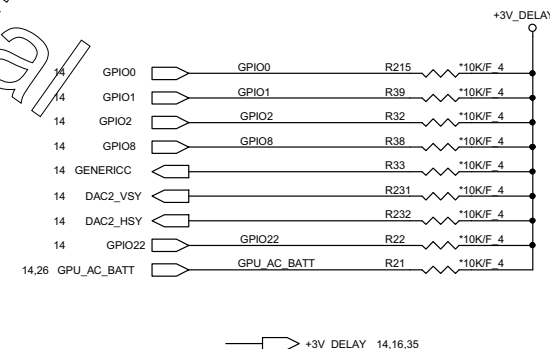
GPIO21 H2SYNC GENERICC GPIO8 GPIO2



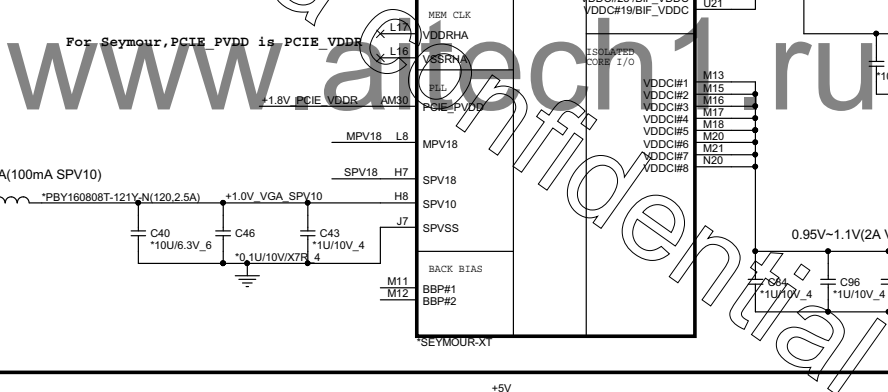
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

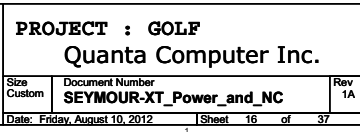
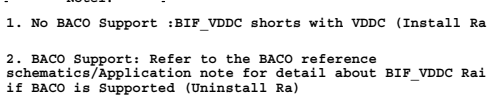
It is a shared pin strap with CONFIG[2:0] if BIOS ROM EN is set to 0.

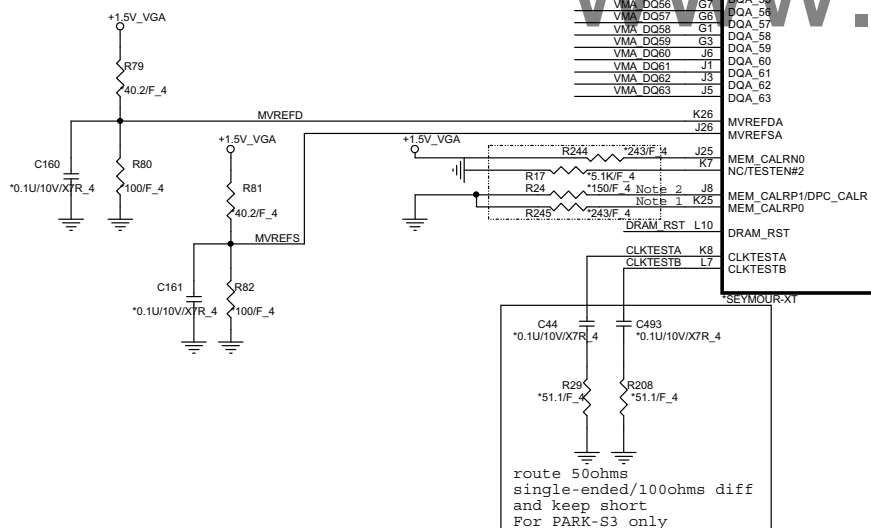
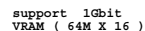


Size Custom	Document Number SEYMOUR-XT GND / LVDS/ Straps	Rev 1A
Date: Friday, August 10, 2012	Sheet 15 of 37	

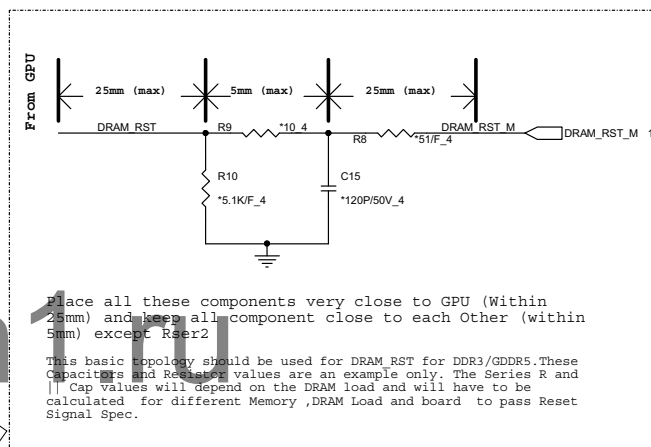


1





U14C

[illegible]

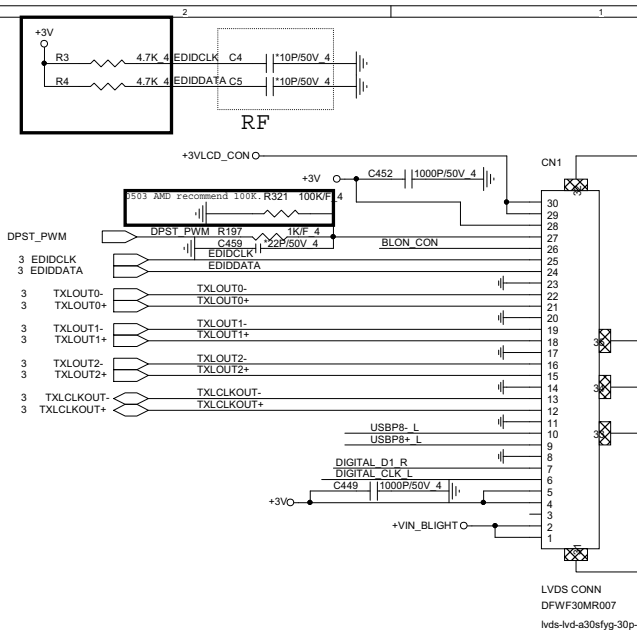
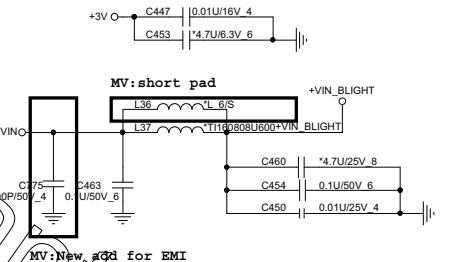
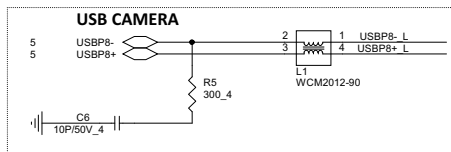
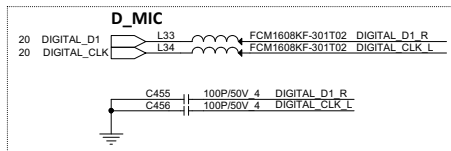
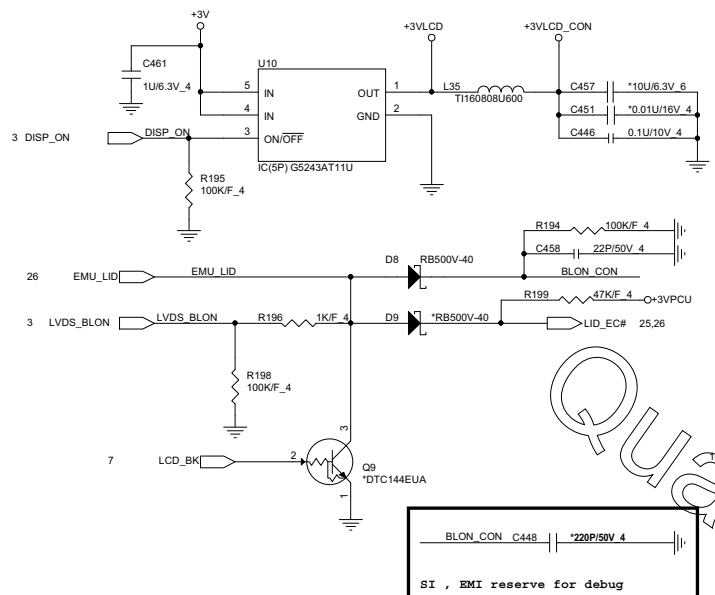


Size	Document Number
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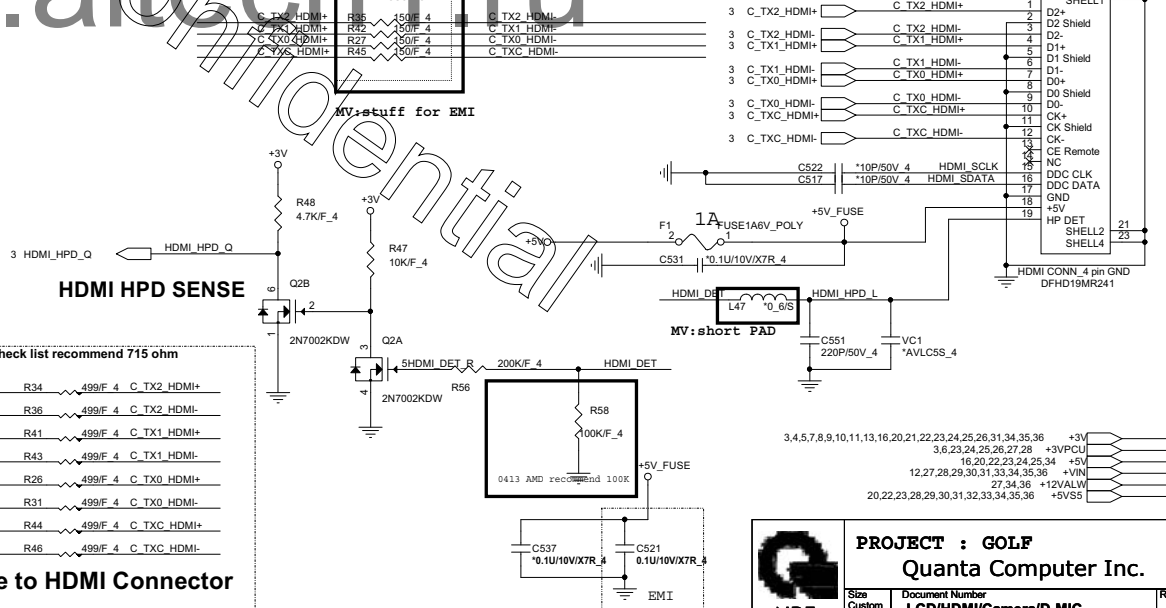
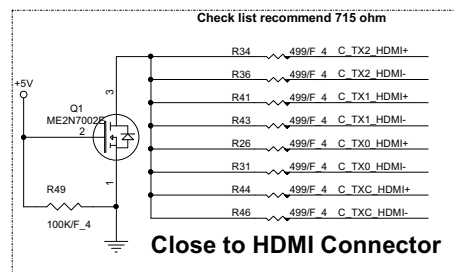
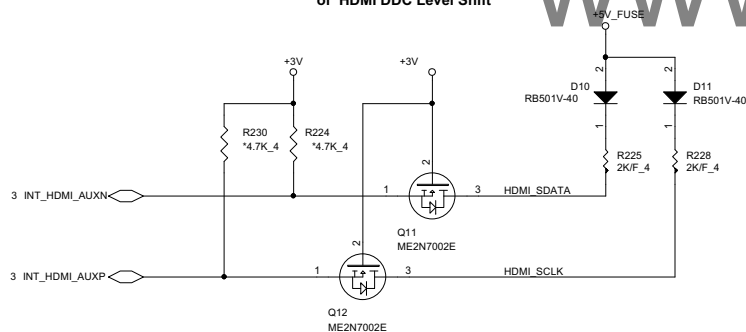
SEYMOUR-XT VRAM(DDR3 BGA96)

Date: Friday, August 10, 2012	Sheet 18 of
-------------------------------	-------------

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LVDS Conn.**HDMI Conn.**

Cost down backup solution of HDMI DDC Level Shift



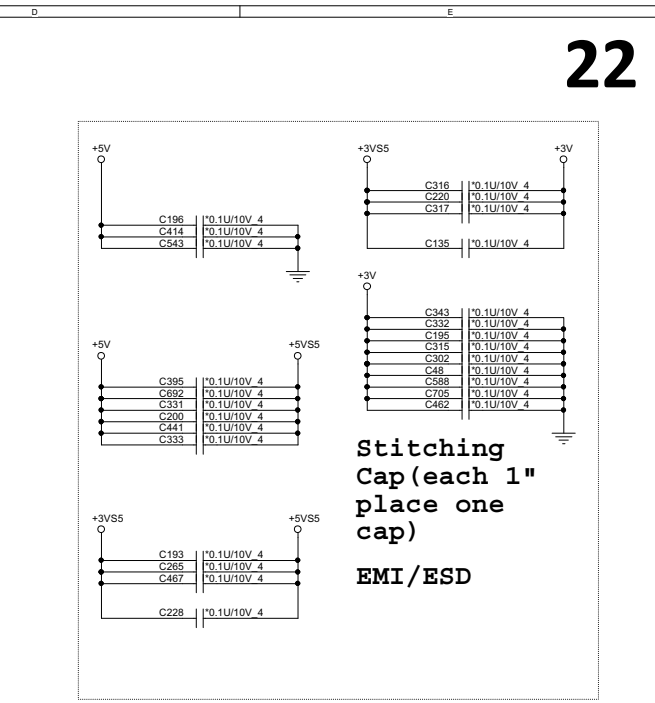
PROJECT : GOLF
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Size Custom	Document Number LCD/HDMI/Camera/D-MIC	Rev 3A
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SD / MMC



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CRT PORT

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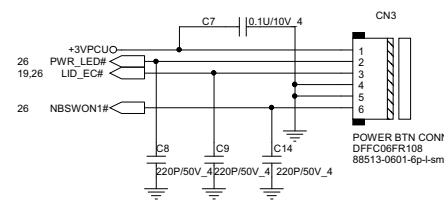


Size Custom	Document Number Card Reader control (RTS5229-GR)
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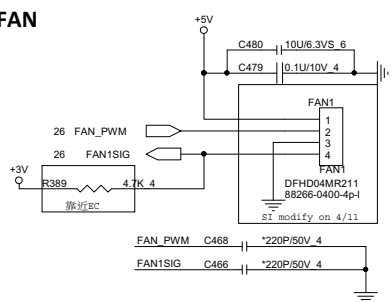
Size Custom	Document Number Card Reader control (RTS5229-GR)	Re
Date: Friday, August 10, 2012	Sheet 22 of 37	

Power Button Connector

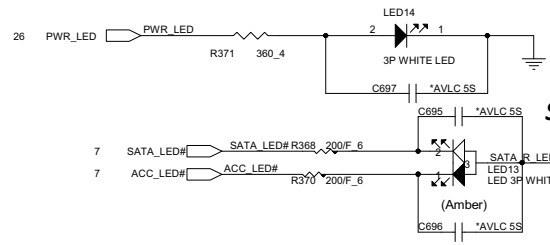
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



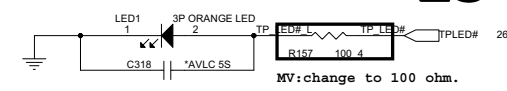
FAN



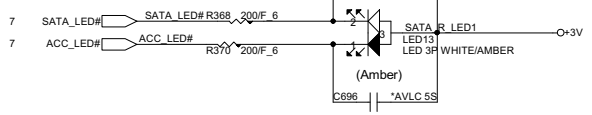
PWR LED



14" TP LED

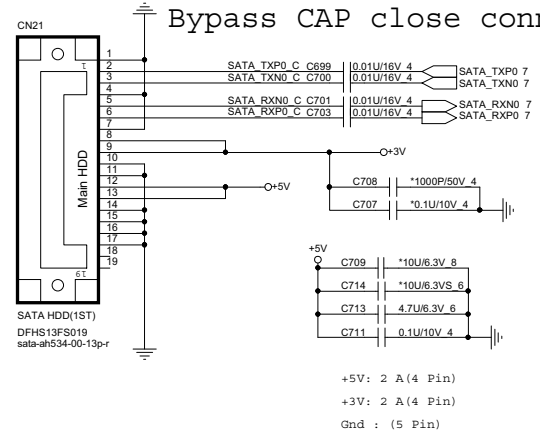


SATA LED

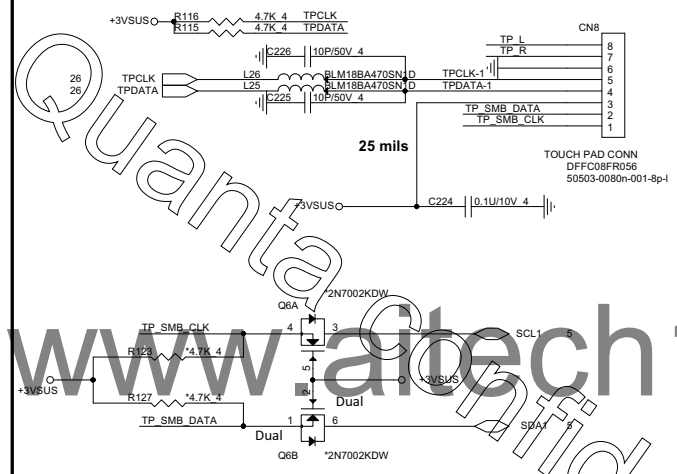


SATA HDD Connector(Cable type)

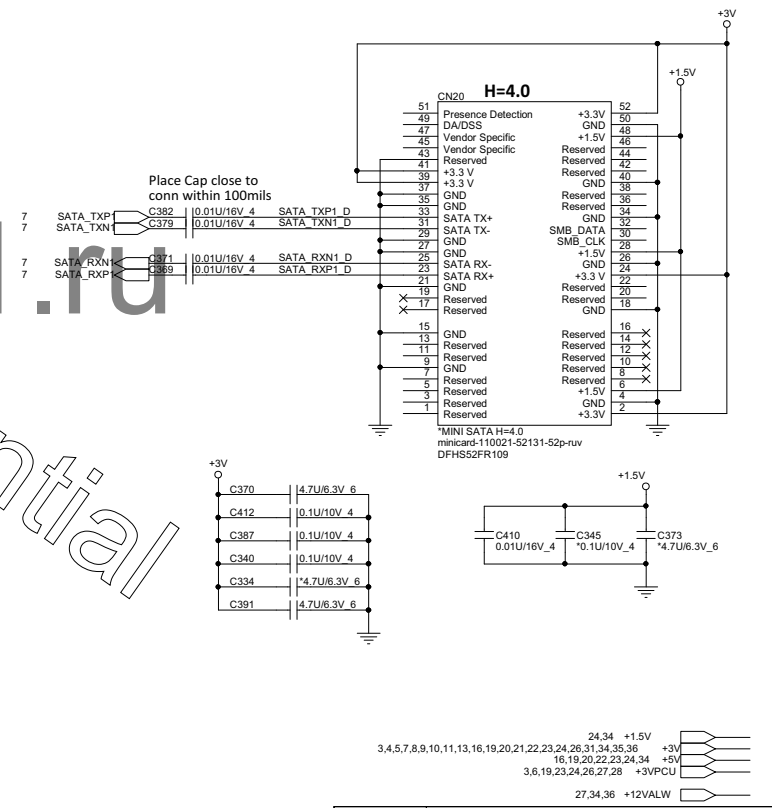
Bypass CAP close conn



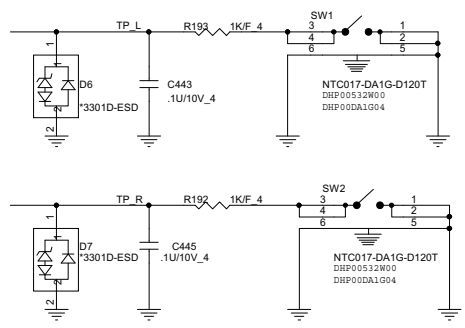
Touch Pad Connector



Mini PCI-E Card 2- Full size mSATA

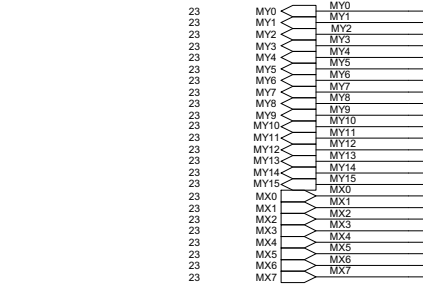
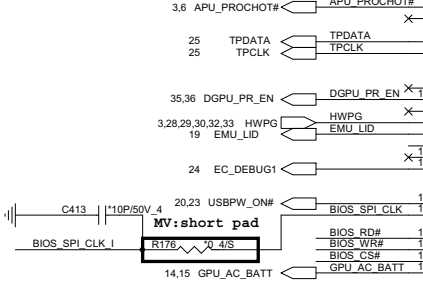
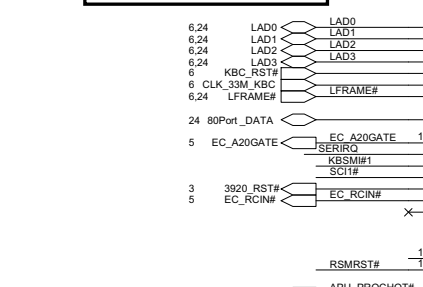
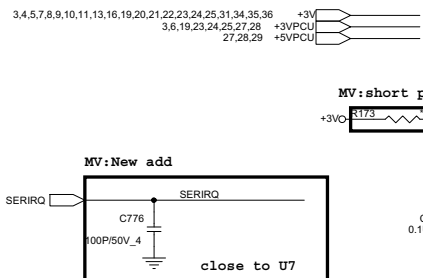


Switch board connector for 15.6"

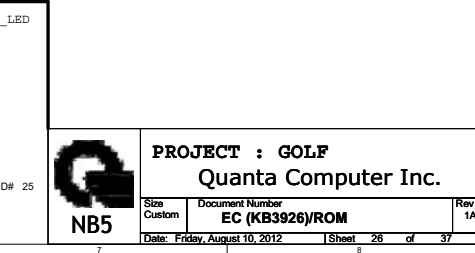
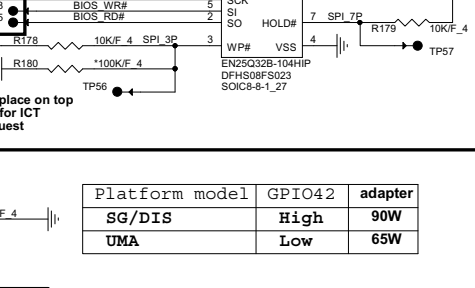
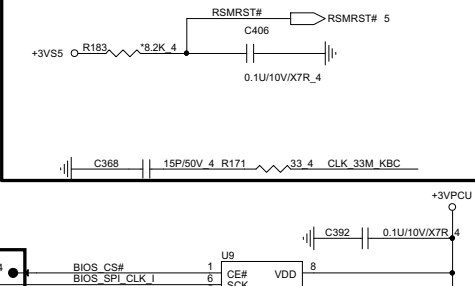
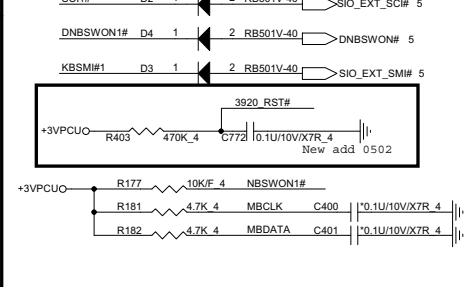
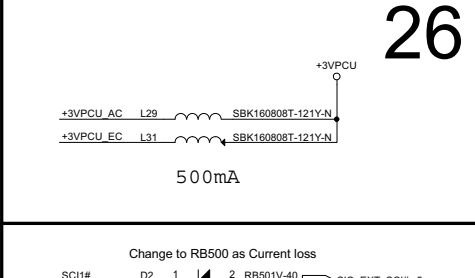
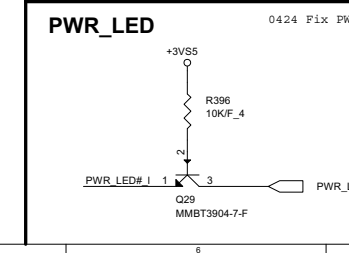
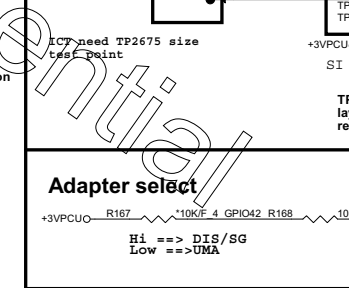
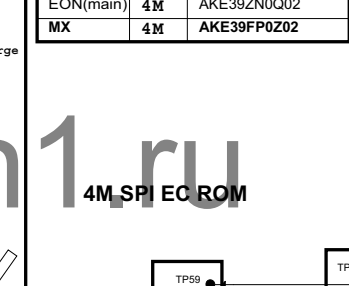
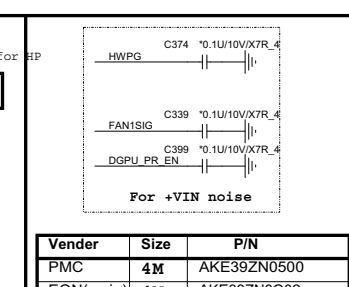
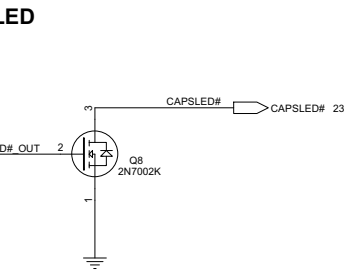
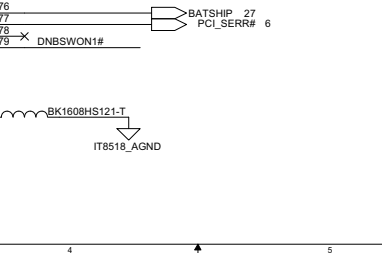
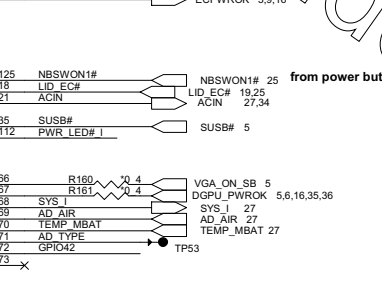
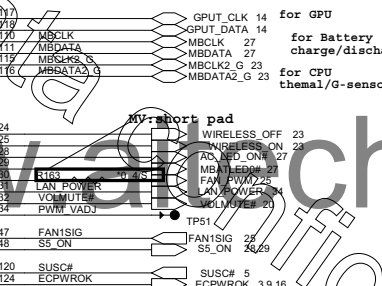
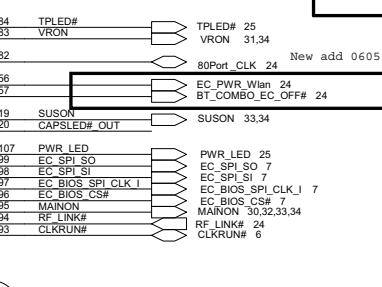
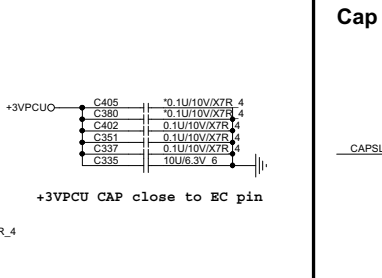
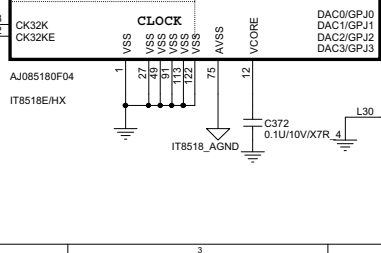
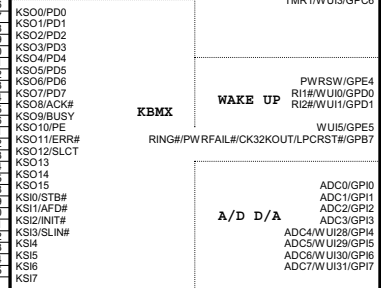
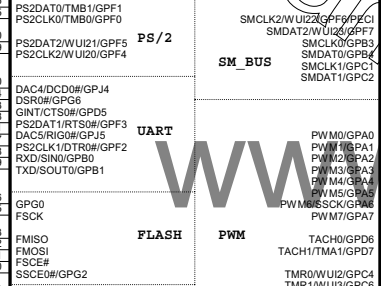
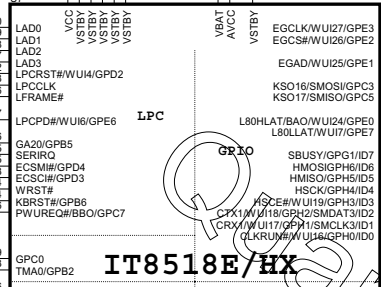
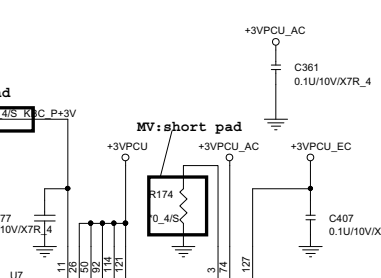


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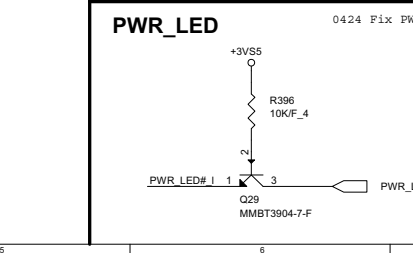
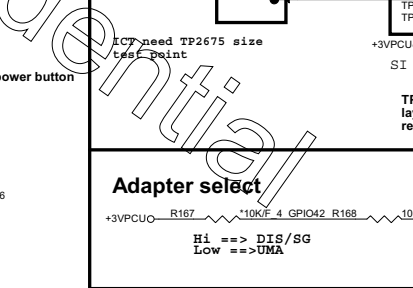
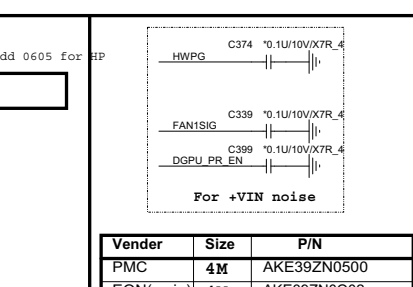
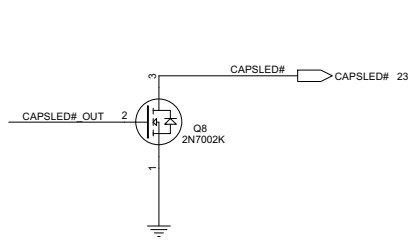
Size Custom	Document Number	Rev A
SATA HDD/ODD/MSATA CONN		
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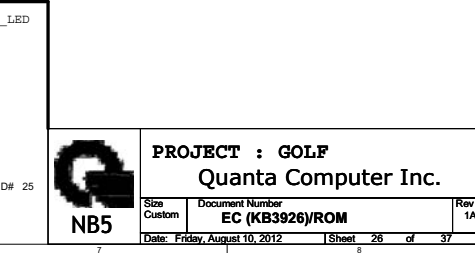
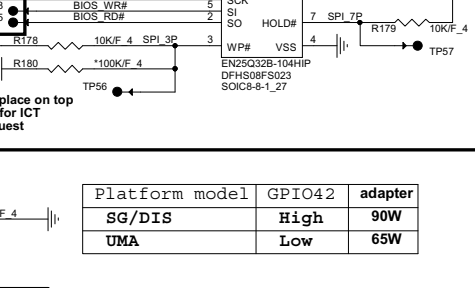
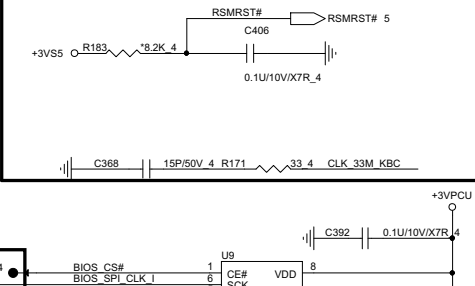
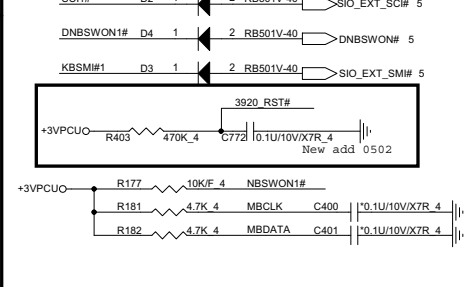
ITE pin 100, 104, 106 default can not pull up to +3VPCU it will cause chip into test mode



Cap LED



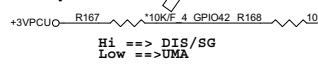
Change to RB500 as Current loss



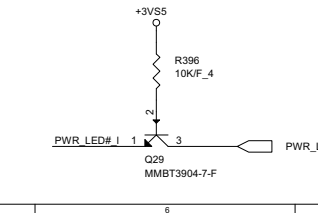
Vender	Size	P/N
PMC	4M	AKE39ZN0500
EON(main)	4M	AKE39ZN0Q02
MX	4M	AKE39FP0Z02

4M SPI EC ROM

Adapter select



PWR_LED

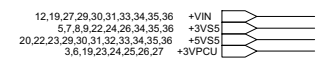


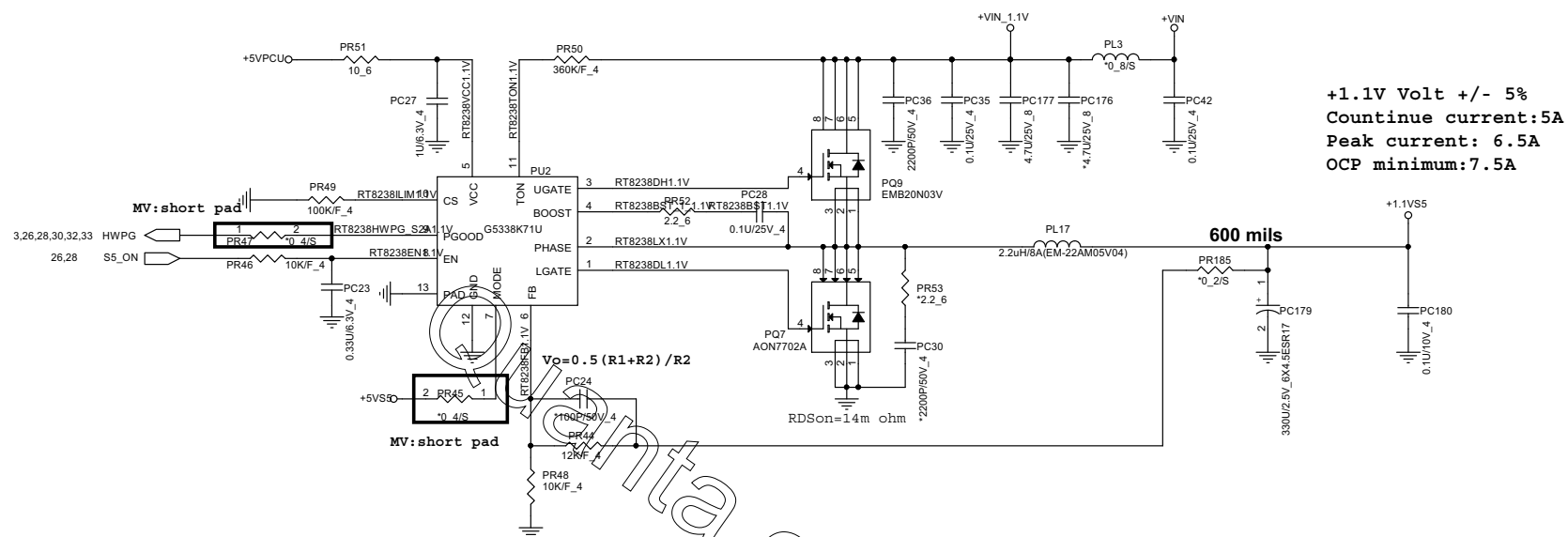
PROJECT : GOLF
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Size	Document Number	Rev
Custom	EC (KB3926)/ROM	1A
Date: Friday, August 10, 2012	Sheet 26 of 37	



Size Custom	Document Number Charger (BQ24728)
Date: Friday, August 10, 2012	Sheet 22 of 22





+1.1V Volt +/- 5%
Continue current:5A
Peak current: 6.5A
OCP minimum:7.5A

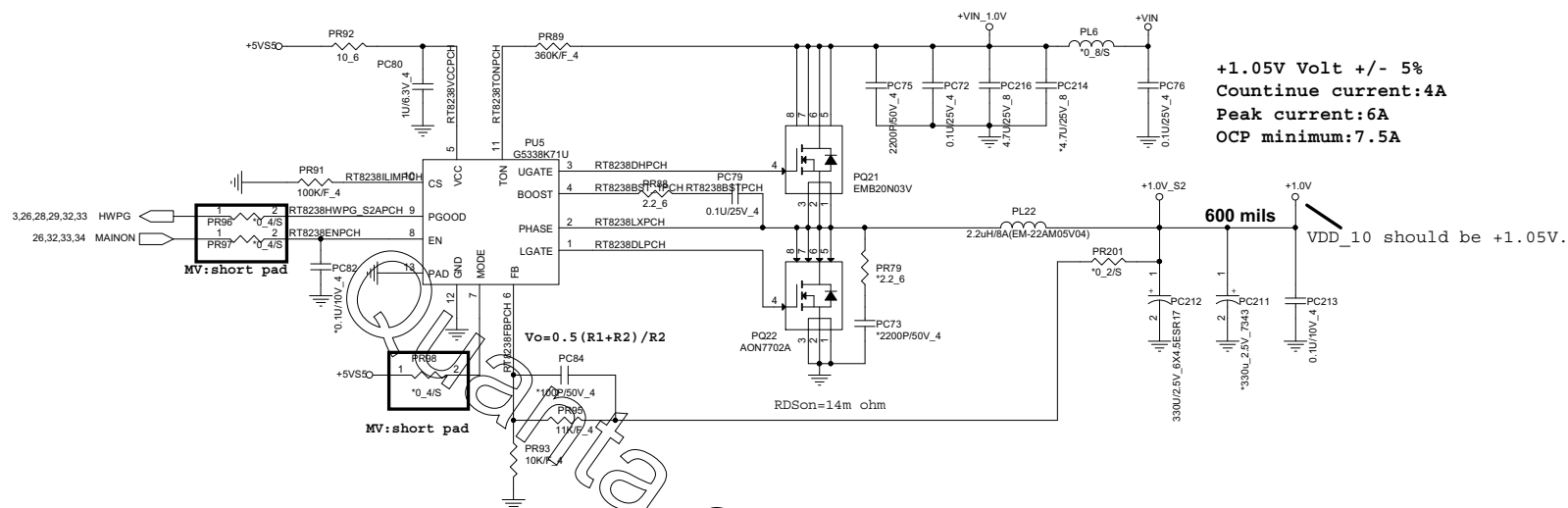
600 mils

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PROJECT : GOLF
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Size Custom	Document Number +1.1VS5 (RT8228)	Rev 1A
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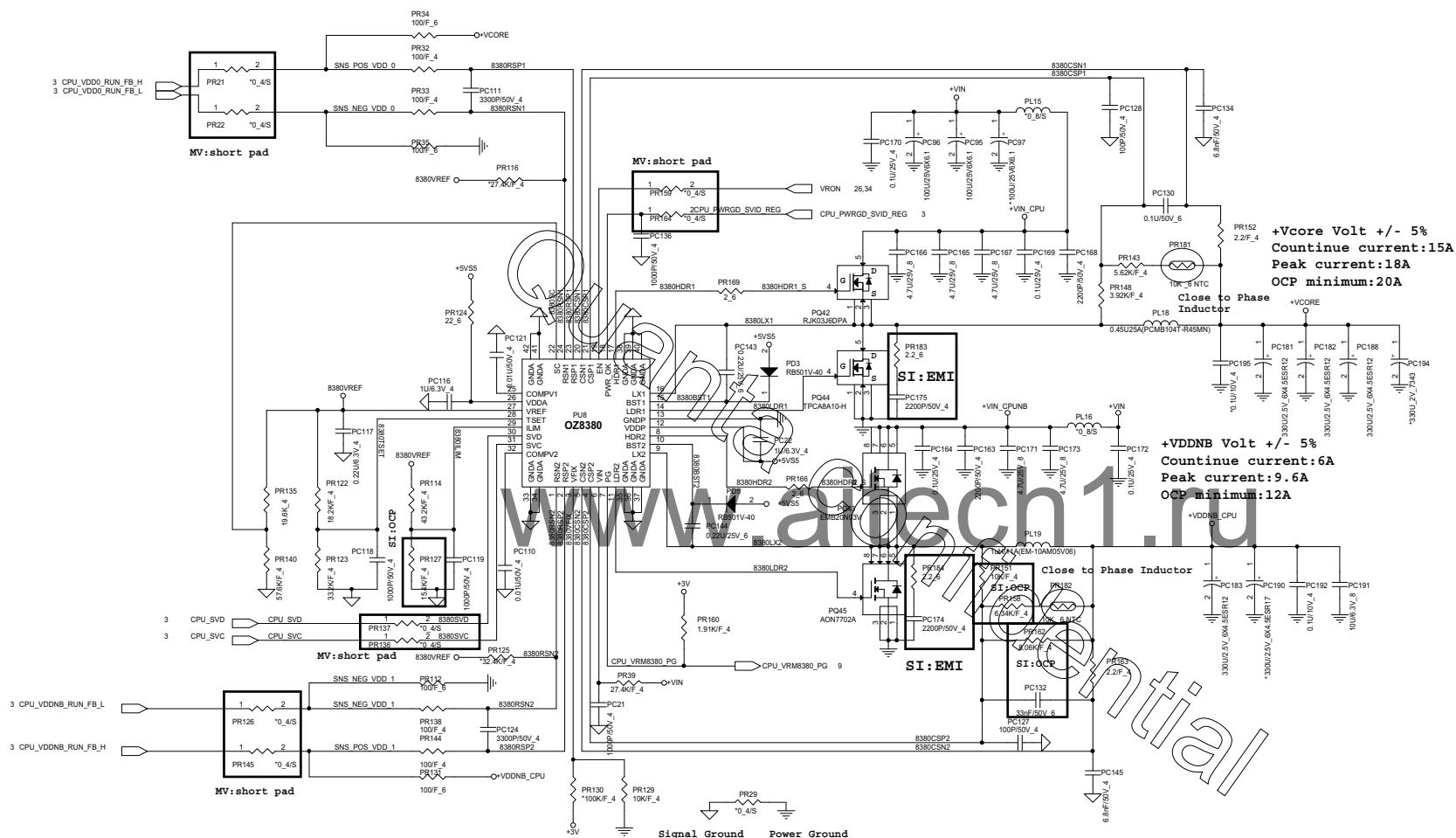


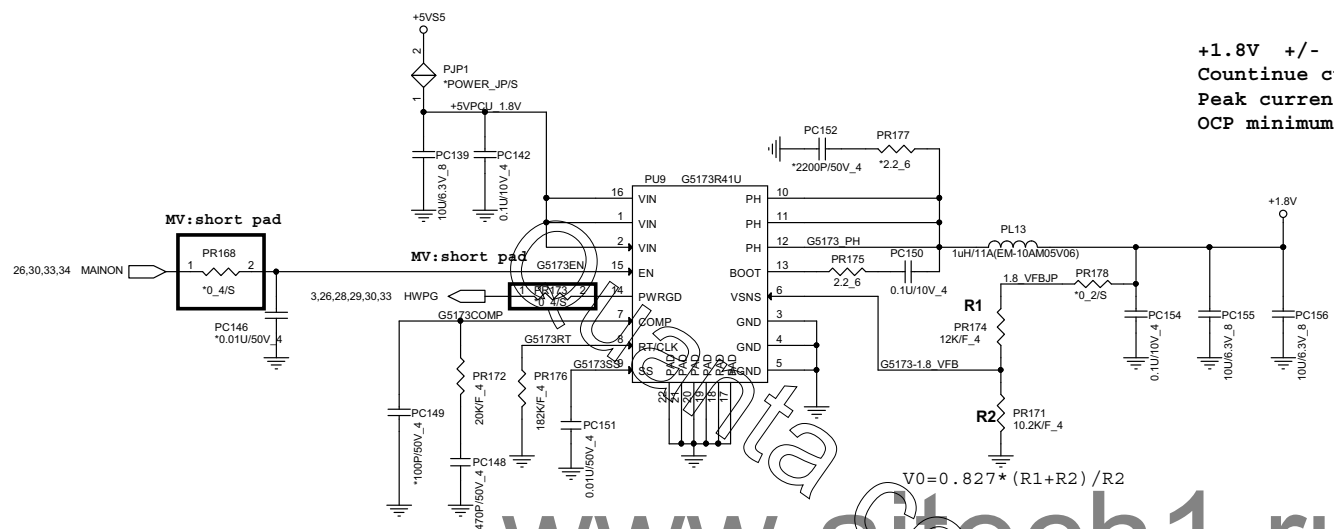
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Size Custom	Document Number +1.0V (RT8228)	Rev 1A
Date: Friday, August 10, 2012	Sheet 30	of 37





$$V_0 = 0.827 \cdot (R_1 + R_2) / R_2$$

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Confidential

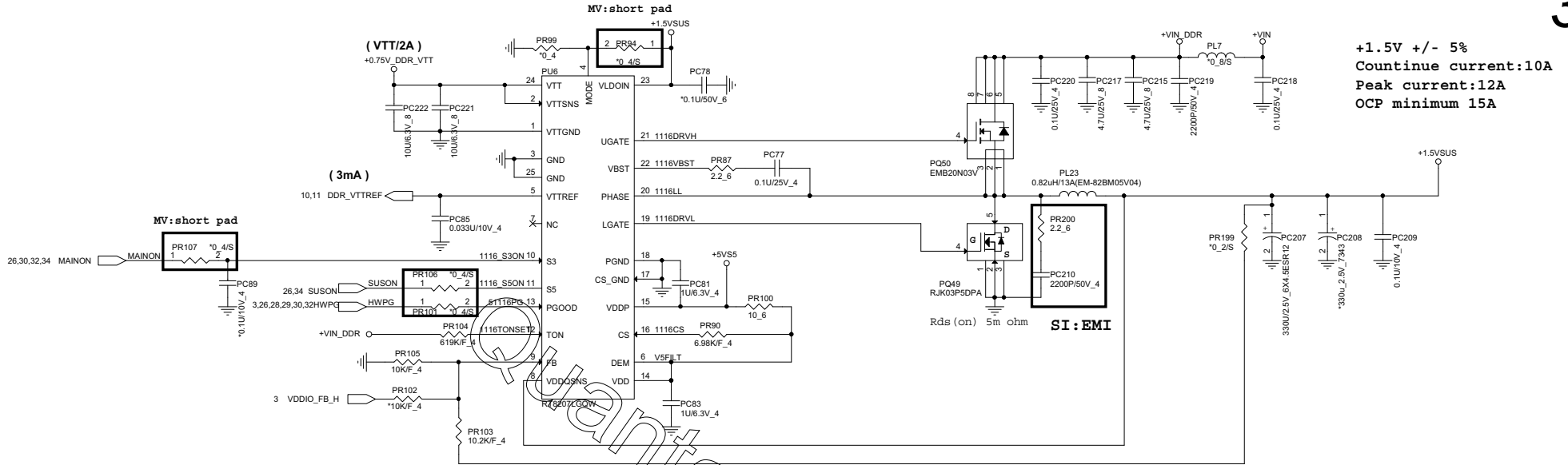


PROJECT : GOLF
Quanta Computer Inc.

Size Custom	Document Number +1.8V (G5173)
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Date: Friday, August 10, 2012	Sheet 32 of 37
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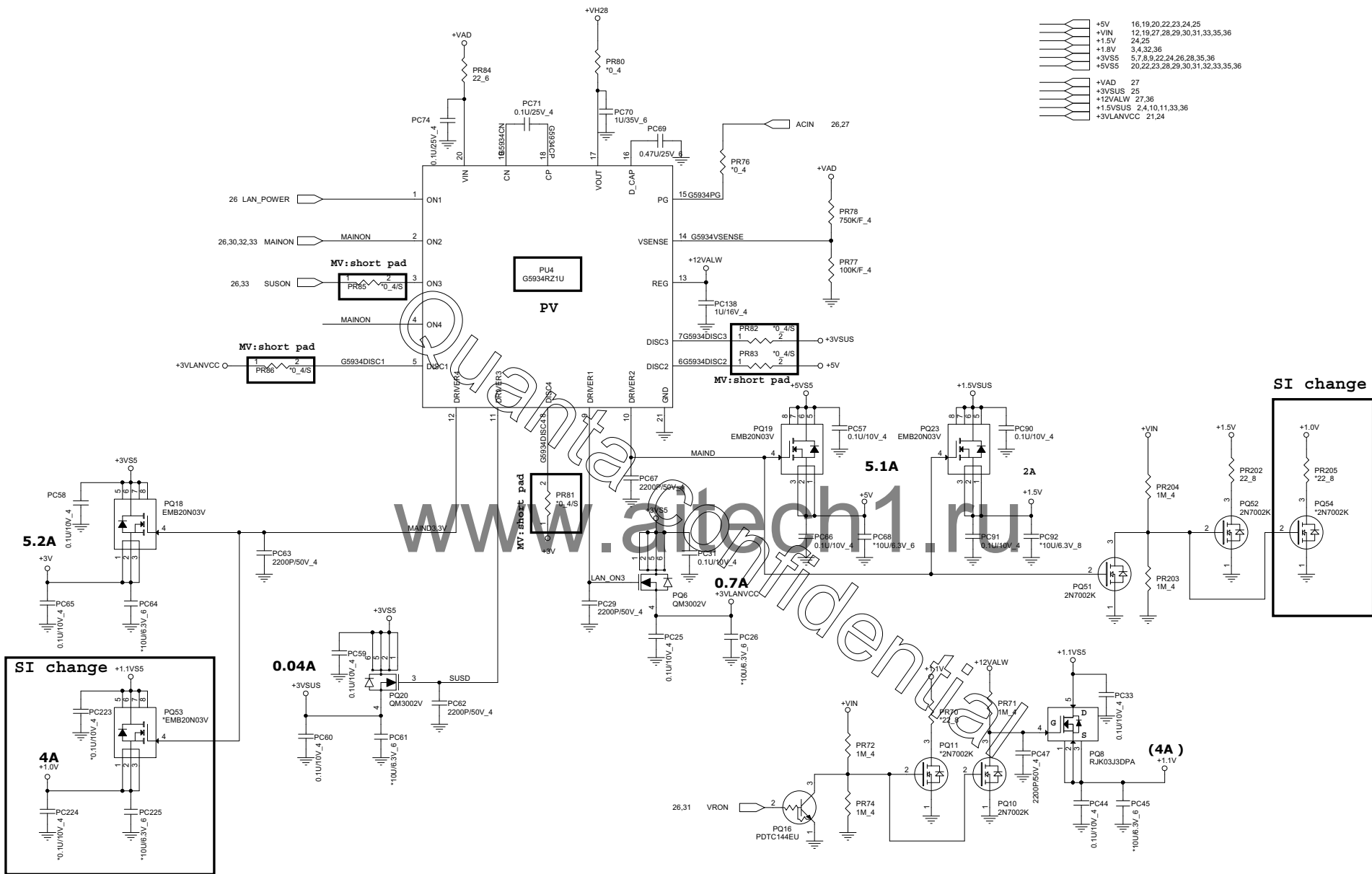


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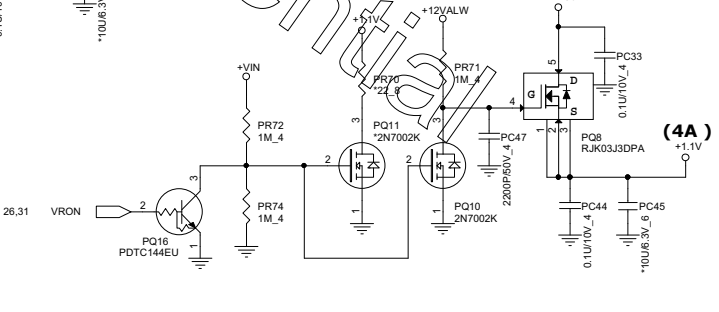
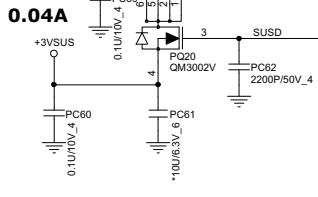
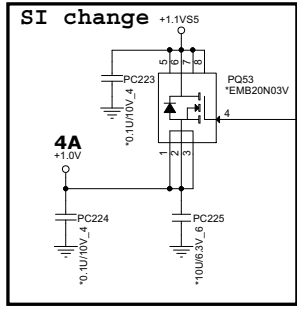
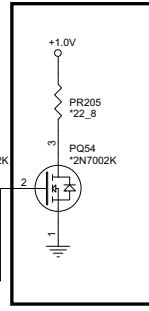
PROJECT : GOLF
Quanta Computer Inc.

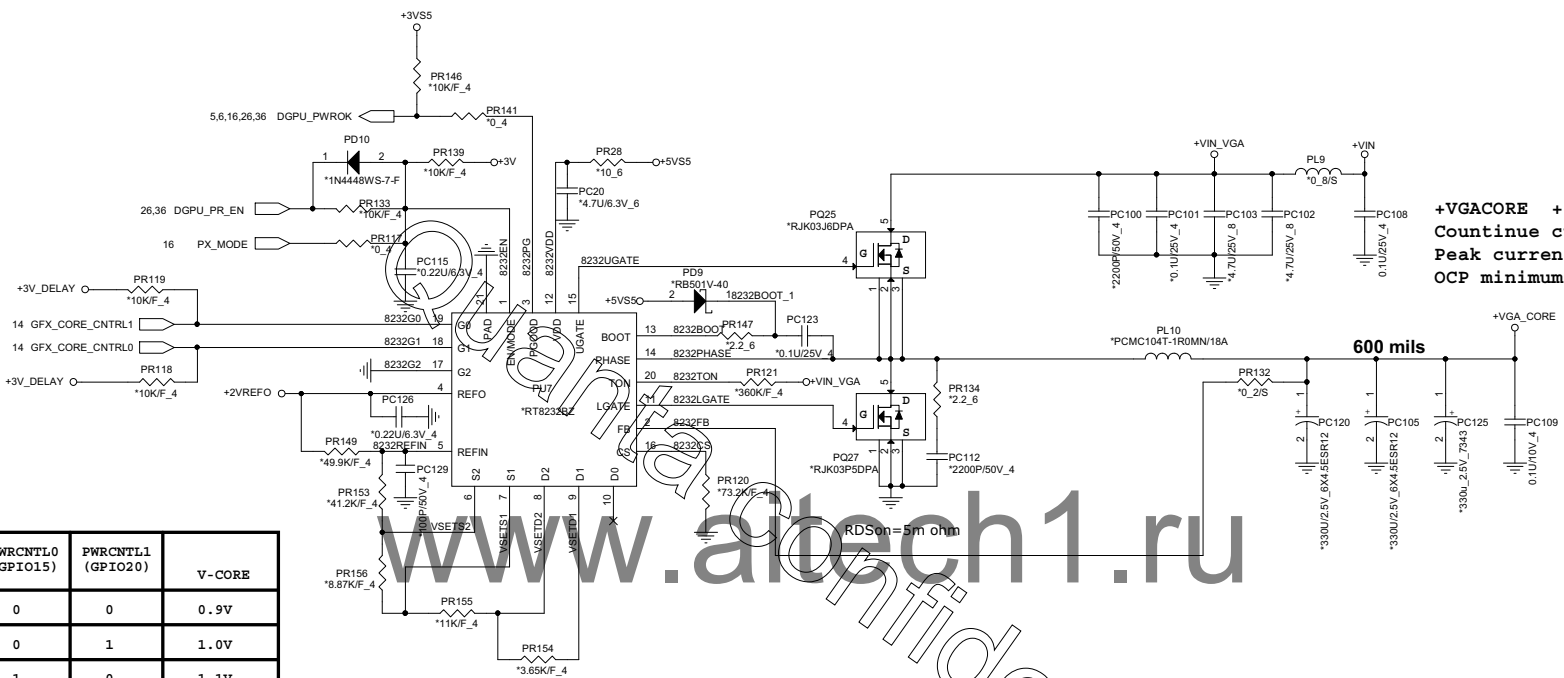
Size Custom	Document Number DDR3(G5616)	Rev 1A
Date: Friday, August 10, 2012	Sheet 33 of 37	



- +5V 16,19,20,22,23,24,25
- +VIN 12,19,27,28,29,30,31,33,35,36
- +1.5V 24,25
- +1.8V 3,4,32,36
- +3VSUS 5,7,8,9,22,24,26,28,35,36
- +5VS5 20,22,23,28,29,30,31,32,33,35,36
- +VAD 27
- +3VSUS 25
- +12VALW 27,36
- +1.5VSUS 2,4,10,11,33,36
- +3VLAVCC 21,24

SI change

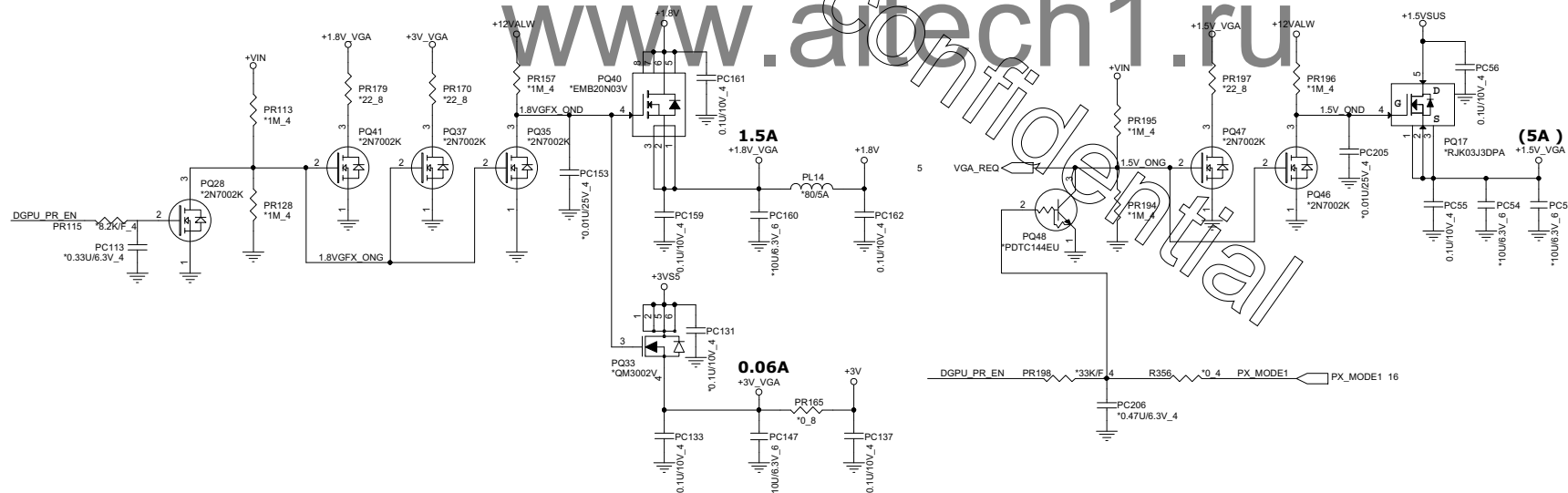
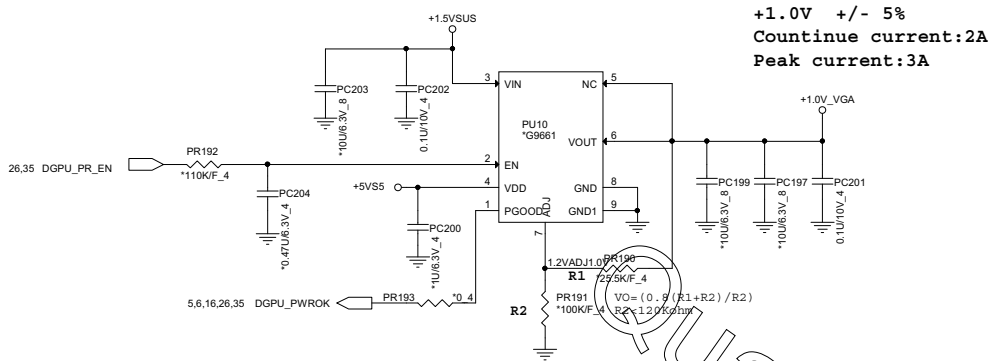




+VGACORE +/- 5%
Countinue current:10.5A
Peak current:11.5A
OCp minimum 16A

Symour-LP	PWRCNTL0 (GPIO15)	PWRCNTL1 (GPIO20)	V-CORE
L	0	0	0.9V
M	0	1	1.0V
H	1	0	1.1V
TBD	1	1	NA

+3V	3,4,5,7,8,9,10,11,13,16,19,20,21,22,23,24,25,26,31,34,35
+VIN	12,19,27,28,29,30,31,33,34,35
+3VS5	5,7,8,9,22,24,26,28,34,35
+5VS5	20,22,23,28,29,30,31,32,33,34,35
+3V_VGA	16
+12VALW	27,34
+1.5VSUS	2,4,10,11,33,34
+1.5V_VGA	16,17,18



PROJECT : GOLF
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Size	Document Number	Rev
Custom	+1.0V_VGA (G5193)	1A
Date:	Friday, August 10, 2012	Sheet 36 of 37

VDDBT_RTC_G
NBSWON1# (EC)
S5_ON
+3VS5/+5VS5
+1.1VS5
RSMRST# (EC -> FCH)
DNBSWON# (EC -> FCH)
SLP_S5# (FCH -> EC)
SLP_S3# (FCH -> EC)
SUSON
+1.5VSUS
MAINON
+1.8/+1.5/1.0/+3/+5
VRON
+VCORE / +VDDNB_CPU
+VCORE PWR GOOD
KBRST# (EC -> FCH)
PWR_GOOD (EC & PWR IC -> FCH)
APU_PG (FCH -> APU)
A_RST# (FCH -> APU)
PCIRST# (FCH -> APU)
APU_RST# (FCH -> APU)



PROJECT : GOLF
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Size Custom	Document Number Sequence	Rev 1A
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